REMARKS

Claims 1-14 and 16-65 are pending in the application. Claims 32-65 are withdrawn from consideration. Claim 15 is cancelled.

Claims 1-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,723,635 to Ngo et al., hereinafter "Ngo", in view of U.S. Patent No. 6,797,605 to Goh et al., hereinafter "Goh". Claim 1 is independent. Claim 15 is cancelled. Applicants respectfully traverse this rejection.

Independent claim 1 provides a dual damascene interconnect structure having a patterned multilayer of dielectrics on a substrate. The multilayer includes a cap layer, a first non-porous via level low-k dielectric layer having thereon metal via conductors with a bottom portion and sidewalls, an etch stop layer, a first porous low-k line level dielectric layer having thereon metal line conductors with a bottom portion and sidewalls, a polish stop layer over said first porous low-k dielectric, a second thin non-porous low-k dielectric layer for coating and planarizing the line and via sidewalls, and a liner material between said metal via and line conductors and said dielectric layers. The second thin non-porous low-k dielectric layer has a composition that is covalently bonded with the first non-porous via level low-k dielectric layer and the first porous low-k line level dielectric layer for enhanced adhesion.

Ngo discloses an multi-level semiconductor device in FIG. 4, including a capping layer 12 such as silicon carbide, first and second porous low-k dielectric layers 13 and 15, a middle etch stop layer 14 (col. 5, lines 34-40). The device also includes a sidewall spacer 30 including a silicon carbide layer 20B and silicon surface region 20A, to prevent degradation of dielectric layers 13 and 15 during deposition of a barrier layer 40 (col. 6, lines 1-5).

Ngo discloses a silicon carbide layer to protect low-k dielectric materials. As admitted by the Office Action, Ngo does not disclose a first non-porous via level low-k dielectric layer, as recited in claim 1.

Also, Ngo merely discloses that the silicon carbide layer lines an opening in the dielectric layers. However, Ngo does not disclose that the silicon surface region 20A is **covalently bonded** with either dielectric layer 13 or 15. Therefore, Ngo does not disclose that "the second thin non-porous low-k dielectric layer has a composition that is covalently bonded with the first non-porous via level low-k dielectric layer and the first porous low-k line level dielectric layer for enhanced adhesion," as recited in claim 1.

Goh discloses a method for improving adhesion of dielectric films. Goh discloses a partially completed integrated circuit device, having a substrate 10, a first low-k dielectric layer 18 deposited over a passivation layer, an etch stop layer deposited over the low-k material layer 18 (col. 2, line 51 – col. 3, line 8). Silicon implantation is disclosed as a means to improve adhesion strength (col. 3, lines 18-25). Silicon implantation roughens the surface of the treated layer (col. 3, lines 33-35). A dual damascene opening is then etched through the first and second dielectric layers, the capping layer and the etch stop layer, using various schemes such as trench-first, via-first, or embedded via (col. 3, lines 53-57).

Goh discloses treating dielectric layers having good adhesion, due to a roughening of a surface of a dielectric layer. However, Goh does not disclose providing a thin non-porous dielectric layer that is **covalently bonded** with a first dielectric layer and a second dielectric layer. Therefore, Goh does not disclose that "the second thin non-porous low-k dielectric layer has a composition that is covalently bonded with the first non-porous via level low-k dielectric layer and the first porous low-k line level dielectric layer for enhanced adhesion," as recited in claim 1.

Neither Ngo nor Goh disclose or suggest a patterned multilayer of dielectrics on a substrate, wherein "the second thin non-porous low-k dielectric layer has a

composition that is covalently bonded with the first non-porous via level low-k dielectric layer and the first porous low-k line level dielectric layer for enhanced adhesion," as recited in claim 1. Therefore, neither Ngo nor Goh, whether considered alone or in combination, disclose or suggest the elements of claim 1. Thus, claim 1 is patentable over the cited combination of Ngo and Goh.

Claims 2-14 and 16-31 depend from claim 1. For at least reasoning similar to that provided in support of the patentability of claim 1, claims 2-14 and 16-31 are patentable over the cited combination of Ngo and Goh.

For the reasons discussed above, the rejection of claims 1-31 under 35 U.S.C. 103(a) as being unpatentable over Ngo in view of Goh is overcome. Applicants respectfully request reconsideration and withdrawal of the rejection of claims 1-31.

An indication of the allowability of all pending claims by issuance of a Notice of Allowability is earnestly solicited.

Respectfully submitted,

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